

Smart High-Side Power Switch

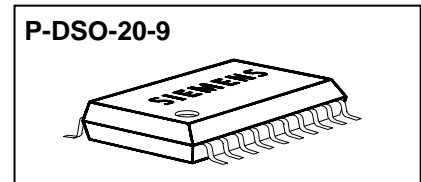
Two Channels: 2 x 60mΩ

Status Feedback

Product Summary

Operating Voltage	$V_{bb(on)}$	4.75...41V	
	Active channels	one	two parallel
On-state Resistance	R_{ON}	60mΩ	30mΩ
Nominal load current	$I_{L(NOM)}$	4.0A	6.0A
Current limitation	$I_{L(SCr)}$	17A	17A

Package



General Description

- N channel vertical power MOSFET with charge pump, ground referenced CMOS compatible input and diagnostic feedback, monolithically integrated in Smart SIPMOS® technology.
- Providing embedded protective functions

Applications

- µC compatible high-side power switch with diagnostic feedback for 5V, 12V and 24V grounded loads
- All types of resistive, inductive and capacitive loads
- Most suitable for loads with high inrush currents, so as lamps
- Replaces electromechanical relays, fuses and discrete circuits

Basic Functions

- Very low standby current
- CMOS compatible input
- Improved electromagnetic compatibility (EMC)
- Fast demagnetization of inductive loads
- Stable behaviour at undervoltage
- Wide operating voltage range
- Logic ground independent from load ground

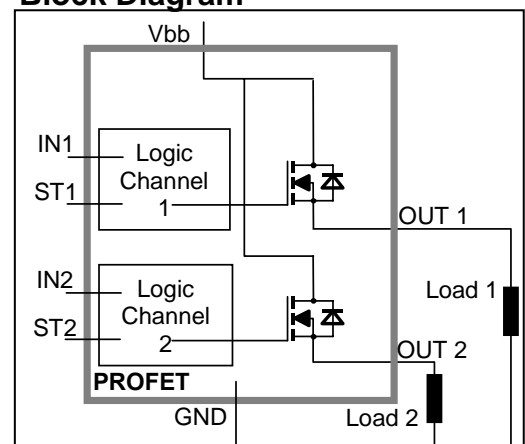
Protection Functions

- Short circuit protection
- Overload protection
- Current limitation
- Thermal shutdown
- Overvoltage protection (including load dump) with external resistor
- Reverse battery protection with external resistor
- Loss of ground and loss of V_{bb} protection
- Electrostatic discharge protection (ESD)

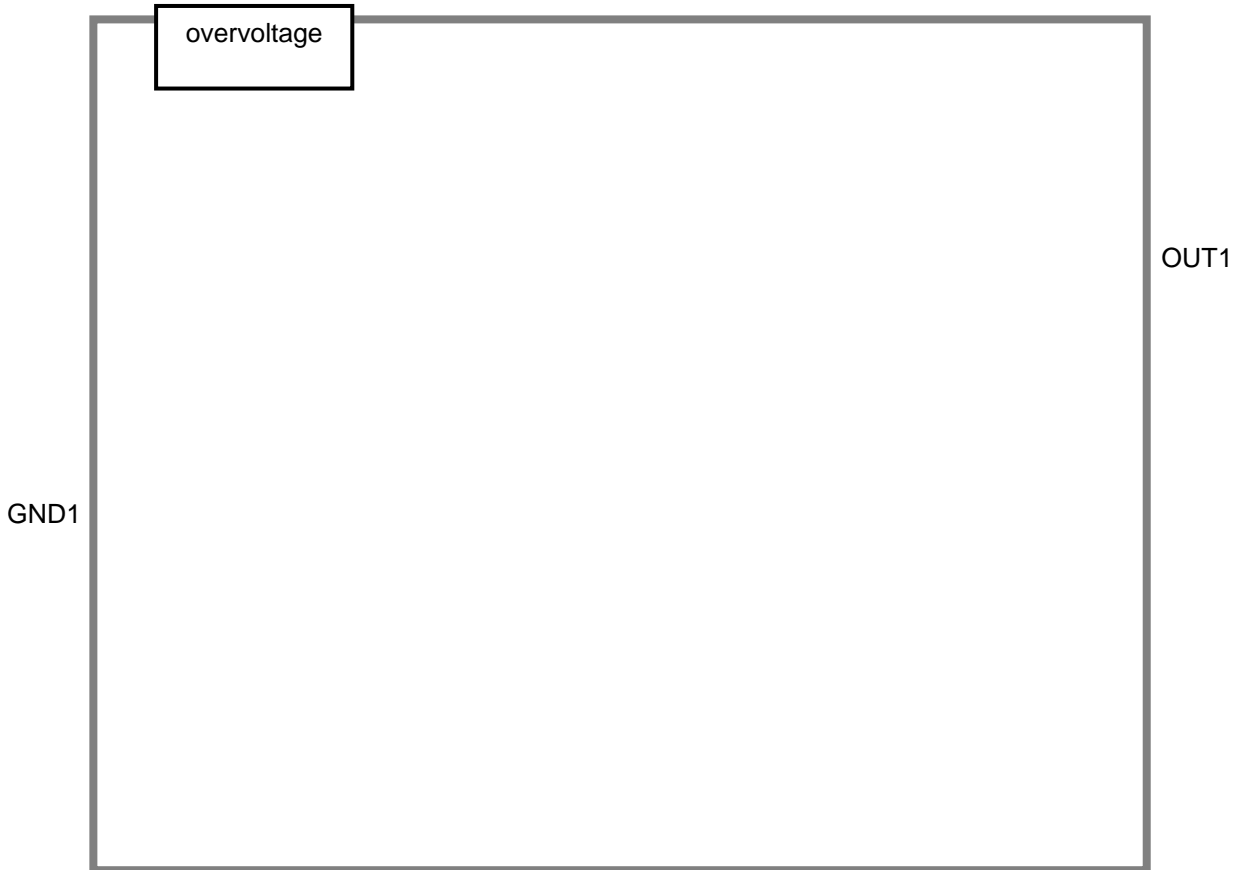
Diagnostic Function

- Diagnostic feedback with open drain output
- Open load detection in ON-state
- Feedback of thermal shutdown in ON-state

Block Diagram



Functional diagram

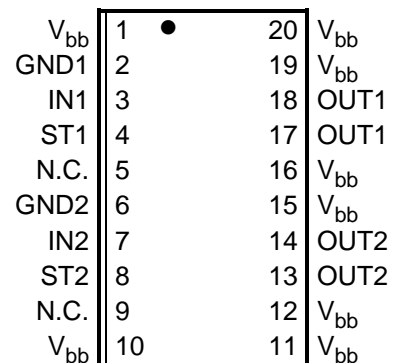


Pin Definitions and Functions

Pin	Symbol	Function
1,10, 11,12, 15,16, 19,20	V_{bb}	Positive power supply voltage. Design the wiring for the simultaneous max. short circuit currents from channel 1 to 2 and also for low thermal resistance
3	IN1	Input 1,2, activates channel 1,2 in case of logic high signal
7	IN2	
17,18	OUT1	Output 1,2, protected high-side power output of channel 1,2. Design the wiring for the max. short circuit current
13,14	OUT2	
4	ST1	Diagnostic feedback 1,2 of channel 1,2, open drain, low on failure
8	ST2	
2	GND1	Ground 1 of chip 1 (channel 1)
6	GND2	Ground 2 of chip 2 (channel 2)
5,9	N.C.	Not Connected

Pin configuration

(top view)



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Parameter and Conditions, each of the two channels at $T_j = -40\dots+150^\circ\text{C}$, $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	Max	

Protection Functions¹²⁾

Current limit, (see timing diagrams, page 12)	$I_{L(\text{lim})}$	$T_j = -40^\circ\text{C}$:	21	28	36	A
		$T_j = 25^\circ\text{C}$:	17	22	31	
		$T_j = +150^\circ\text{C}$:	12	16	24	
Repetitive short circuit current limit, $T_j = T_{jt}$ each channel two parallel channels (see timing diagrams, page 12)	$I_{L(\text{SCR})}$		--	17	--	A
			--	17	--	
Initial short circuit shutdown time $T_{j,\text{start}} = 25^\circ\text{C}$: (see timing diagrams on page 12)	$t_{\text{off}(\text{SC})}$		--	2.4	--	ms
Output clamp (inductive load switch off) ¹³⁾ at $V_{\text{ON}(\text{CL})} = V_{bb} - V_{\text{OUT}}$, $I_L = 40\text{ mA}$	$V_{\text{ON}(\text{CL})}$	$T_j = -40^\circ\text{C}$:	41	--	--	V
		$T_j = 25^\circ\text{C}\dots150^\circ\text{C}$:	43	47	52	
Thermal overload trip temperature	T_{jt}		150	--	--	$^\circ\text{C}$
Thermal hysteresis	ΔT_{jt}		--	10	--	K

Reverse Battery

Reverse battery voltage ¹⁴⁾	$-V_{bb}$	--	--	32	V
Drain-source diode voltage ($V_{\text{out}} > V_{bb}$) $I_L = -4.0\text{ A}$, $T_j = +150^\circ\text{C}$	$-V_{\text{ON}}$	--	600	--	mV

¹²⁾ Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

¹³⁾ If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest $V_{\text{ON}(\text{CL})}$



¹⁴⁾ Requires a 150 Ω resistor in GND connection. The reverse load current through the intrinsic drain-source diode has to be limited by the connected load. Power dissipation is higher compared to normal operating conditions due to the voltage drop across the drain-source diode. The temperature protection is not active during reverse current operation! Input and Status currents have to be limited (see max. ratings page 3 and circuit page 8).

Parameter and Conditions, each of the two channels at $T_j = -40\dots+150^\circ\text{C}$, $V_{bb} = 12\text{ V}$ unless otherwise specified	Symbol	Values			Unit
		min	typ	Max	

Diagnostic Characteristics

Open load detection current, (on-condition) each channel	$I_{L(OL)}$	10	--	500	mA
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Input and Status Feedback¹⁵⁾

Input resistance (see circuit page 8)	R_I	2.5	3.5	6	k Ω
Input turn-on threshold voltage 	$V_{IN(T+)}$	1.7	--	3.2	V
Input turn-off threshold voltage 	$V_{IN(T-)}$	1.5	--	--	V
Input threshold hysteresis	$\Delta V_{IN(T)}$	--	0.5	--	V
Off state input current $V_{IN} = 0.4\text{ V}$:	$I_{IN(off)}$	1	--	50	μA
On state input current $V_{IN} = 5\text{ V}$:	$I_{IN(on)}$	20	50	90	μA
Delay time for status with open load after switch off; (see diagram on page 13)	$t_{d(ST\ OL4)}$	100	520	900	μs
Status invalid after positive input slope (open load)	$t_{d(ST)}$	--	--	500	μs
Status output (open drain)					
Zener limit voltage $I_{ST} = +1.6\text{ mA}$:	$V_{ST(high)}$	5.4	6.1	--	V
ST low voltage $I_{ST} = +1.6\text{ mA}$:	$V_{ST(low)}$	--	--	0.4	

¹⁵⁾ If ground resistors R_{GND} are used, add the voltage drop across these resistors.

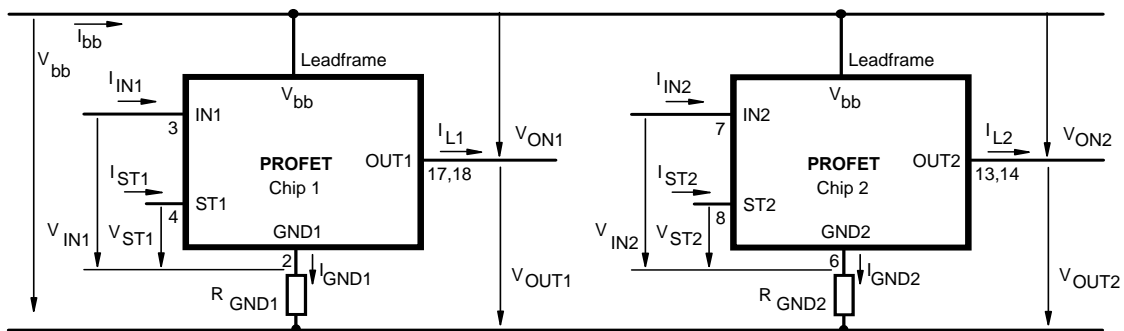
Truth Table

Channel 1	Input 1	Output 1	Status 1
Channel 2	Input 2	Output 2	Status 2
	level	level	BTS 728L2
Normal operation	L	L	H
	H	H	H
Open load	L	Z	H
	H	H	L
Overtemperature	L	L	H
	H	L	L

L = "Low" Level X = don't care Z = high impedance, potential depends on external circuit
H = "High" Level Status signal valid after the time delay shown in the timing diagrams

Parallel switching of channel 1 and 2 is easily possible by connecting the inputs and outputs in parallel. The status outputs ST1 and ST2 have to be configured as a 'Wired OR' function with a single pull-up resistor.

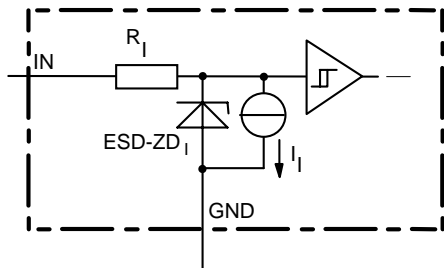
Terms



Leadframe (V_{bb}) is connected to pin 1,10,11,12,15,16,19,20

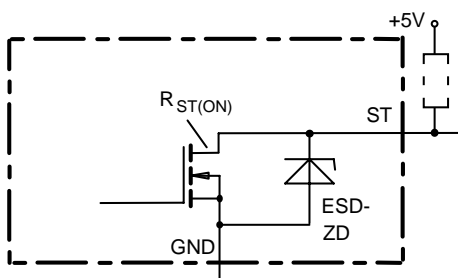
External R_{GND} optional; two resistors R_{GND1} , $R_{GND2} = 150 \Omega$ or a single resistor $R_{GND} = 75 \Omega$ for reverse battery protection up to the max. operating voltage.

Input circuit (ESD protection), IN1 or IN2



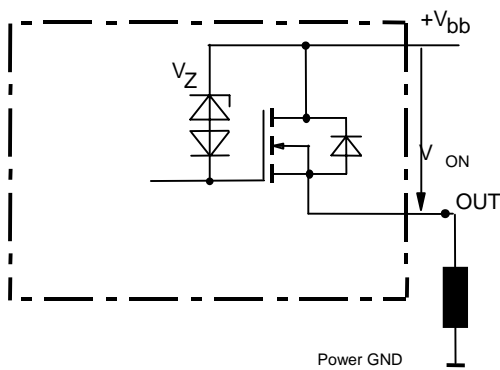
The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

Status output, ST1 or ST2



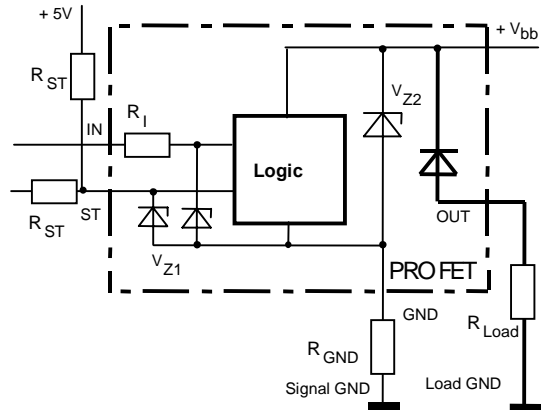
ESD-Zener diode: 6.1 V typ., max 5.0 mA; $R_{ST(ON)} < 375 \Omega$ at 1.6 mA. The use of ESD zener diodes as voltage clamp at DC conditions is not recommended.

Inductive and overvoltage output clamp, OUT1 or OUT2



V_{ON} clamped to $V_{ON(CL)} = 47 \text{ V typ.}$

Overvolt. and reverse batt. protection



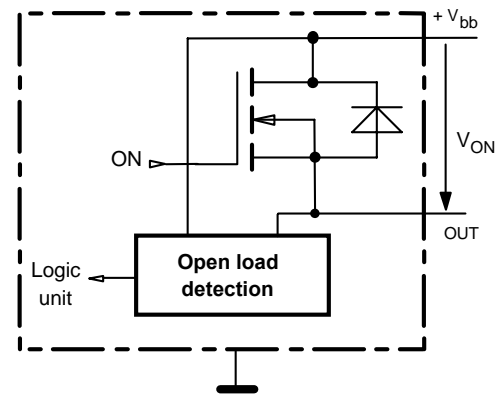
$V_{Z1} = 6.1 \text{ V typ.}$, $V_{Z2} = 47 \text{ V typ.}$, $R_{GND} = 150 \Omega$, $R_{ST} = 15 \text{ k}\Omega$, $R_I = 3.5 \text{ k}\Omega \text{ typ.}$

In case of reverse battery the load current has to be limited by the load. Temperature protection is not active

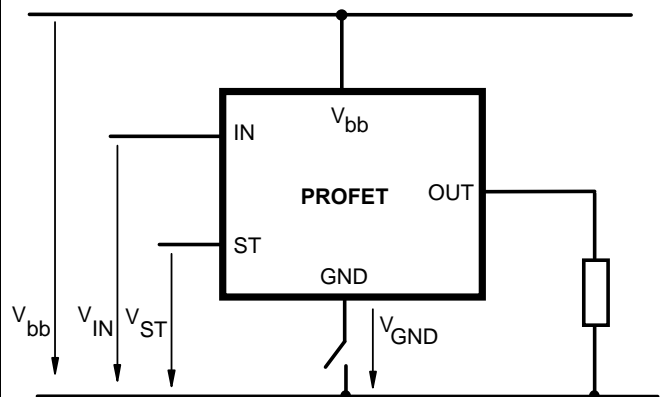
Open-load detection OUT1 or OUT2

ON-state diagnostic

Open load, if $V_{ON} < R_{ON} \cdot I_{L(OL)}$; IN high

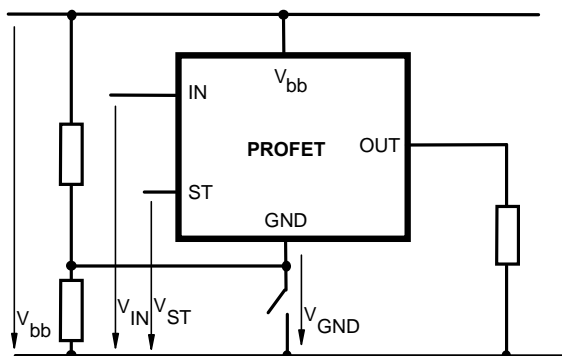


GND disconnect



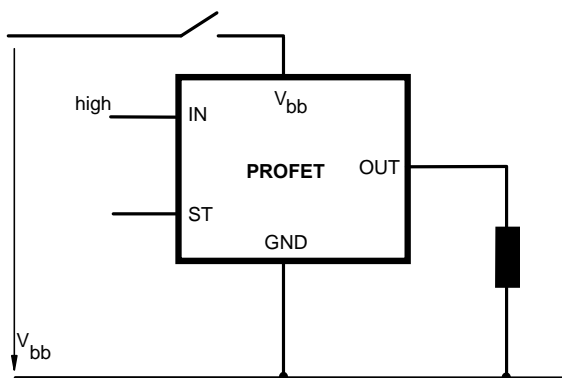
Any kind of load. In case of IN=high is $V_{OUT} \approx V_{IN} - V_{IN(T+)}$. Due to $V_{GND} > 0$, no $V_{ST} = \text{low}$ signal available.

GND disconnect with GND pull up



Any kind of load. If $V_{GND} > V_{IN} - V_{IN(T+)}$ device stays off
 Due to $V_{GND} > 0$, no $V_{ST} = \text{low}$ signal available.

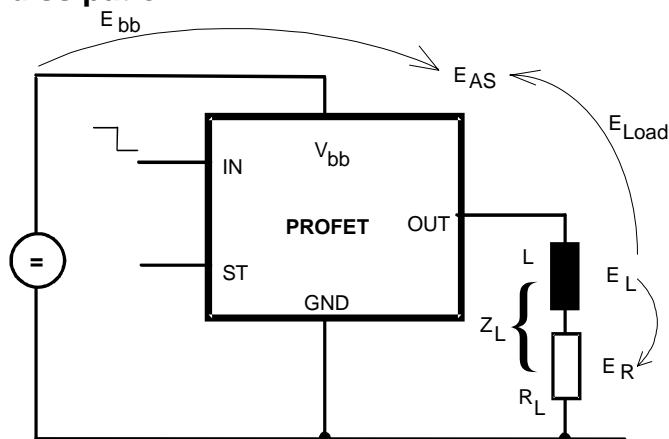
Vbb disconnect with energized inductive load



For inductive load currents up to the limits defined by Z_L (max. ratings and diagram on page 9) each switch is protected against loss of V_{bb} .

Consider at your PCB layout that in the case of V_{bb} disconnection with energized inductive load all the load current flows through the GND connection.

Inductive load switch-off energy dissipation



Energy stored in load inductance:

$$E_L = 1/2 \cdot L \cdot I_L^2$$

While demagnetizing load inductance, the energy dissipated in PROFET is

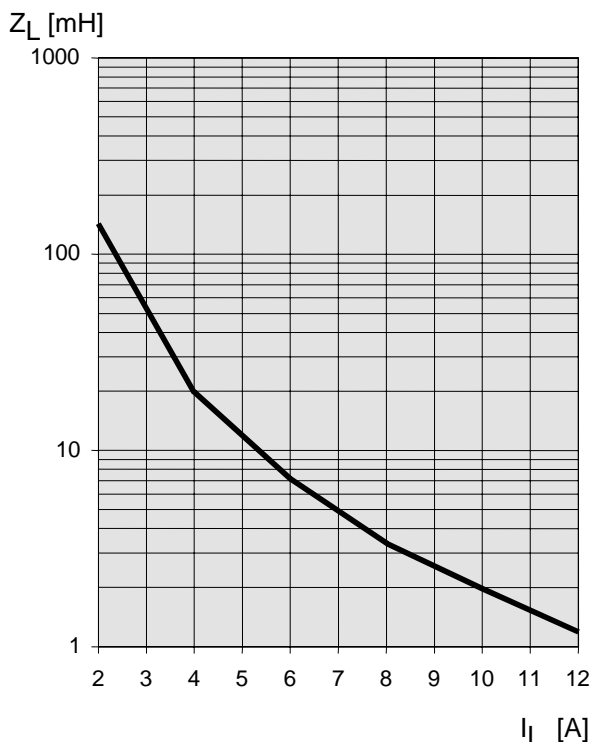
$$E_{AS} = E_{bb} + E_L - E_R = V_{ON(CL)} \cdot i_L(t) dt,$$

with an approximate solution for $R_L > 0\Omega$:

$$E_{AS} = \frac{I_L \cdot L}{2 \cdot R_L} (V_{bb} + |V_{OUT(CL)}|) \ln \left(1 + \frac{I_L \cdot R_L}{|V_{OUT(CL)}|} \right)$$

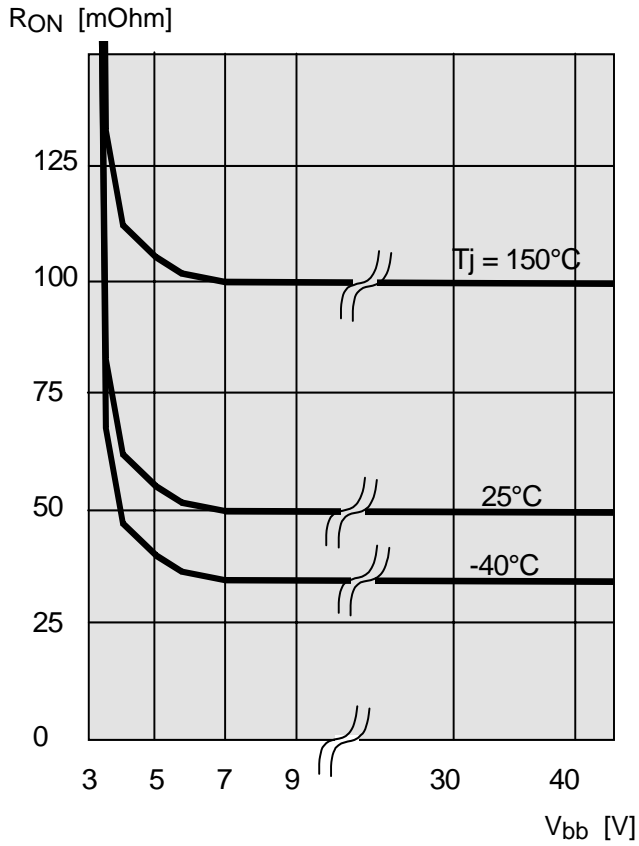
Maximum allowable load inductance for a single switch off (one channel)⁴⁾

$$L = f(I_L); T_{j,start} = 150^\circ\text{C}, V_{bb} = 12\text{V}, R_L = 0\Omega$$



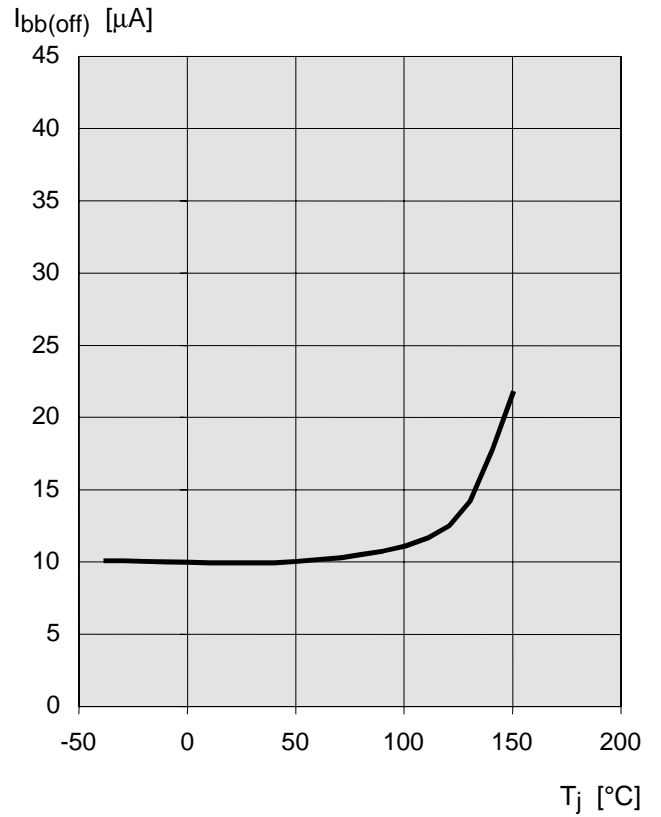
Typ. on-state resistance

$R_{ON} = f(V_{bb}, T_j)$; $I_L = 2\text{ A}$, $I_N = \text{high}$



Typ. standby current

$I_{bb(off)} = f(T_j)$; $V_{bb} = 9 \dots 34\text{ V}$, $I_{N1,2} = \text{low}$



Timing diagrams

Both channels are symmetric and consequently the diagrams are valid for channel 1 and channel 2

Figure 1a: V_{bb} turn on:

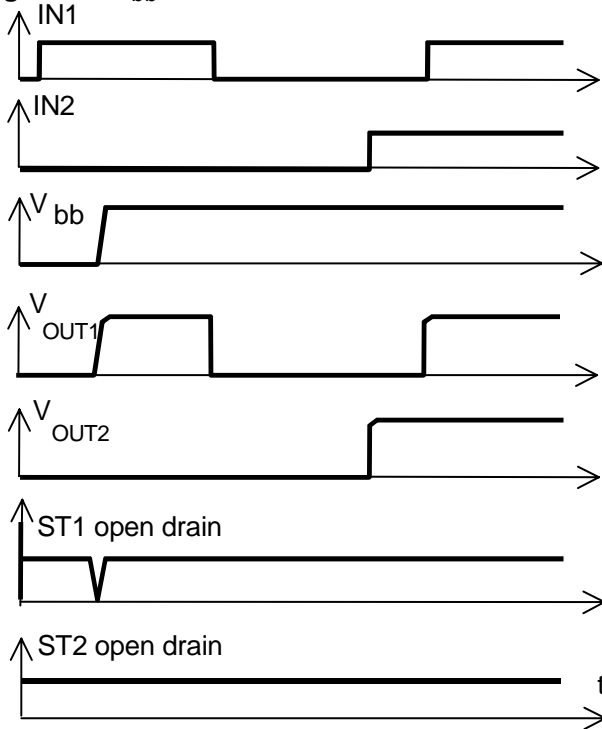
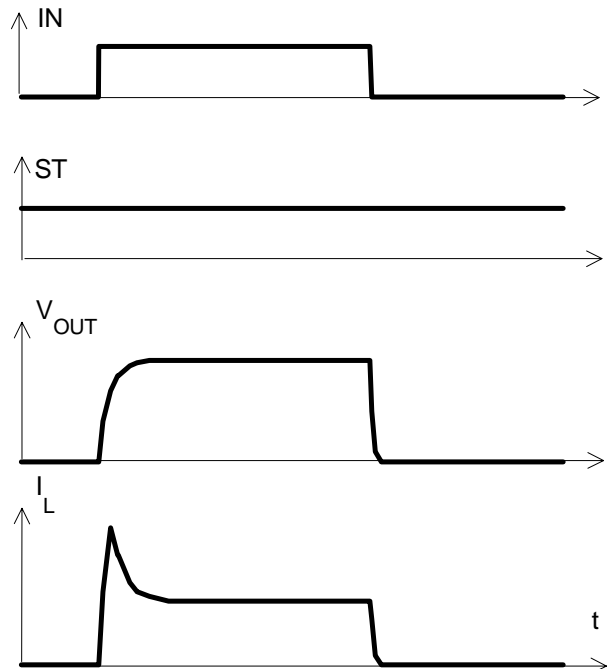


Figure 2b: Switching a lamp:



The initial peak current should be limited by the lamp and not by the current limit of the device.

Figure 2a: Switching a resistive load, turn-on/off time and slew rate definition:

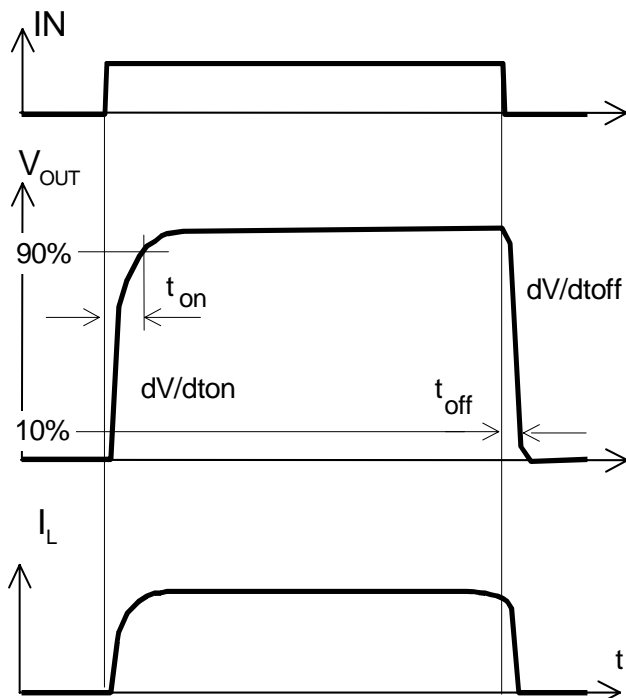
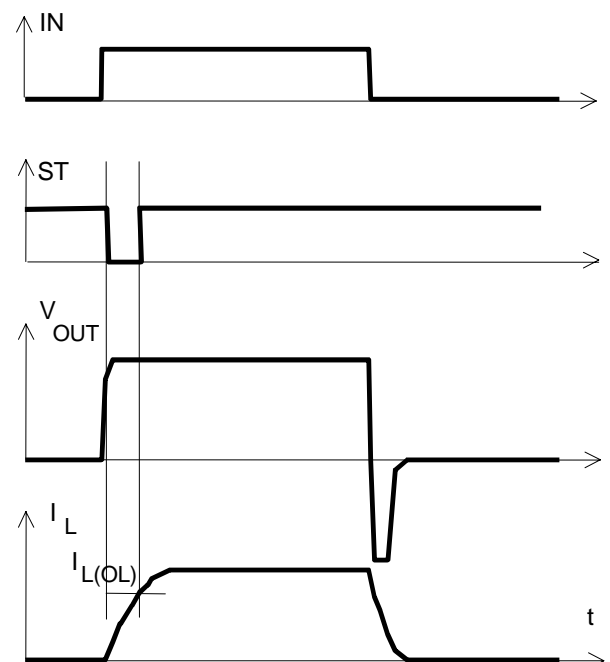
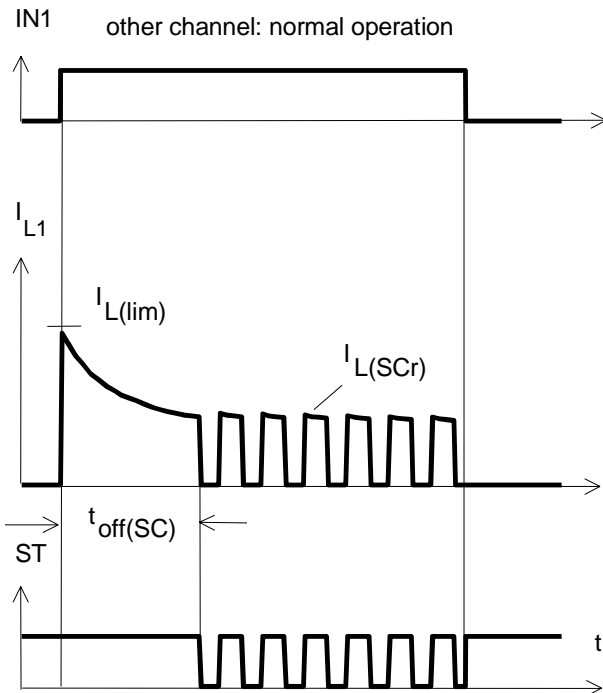


Figure 2c: Switching an inductive load



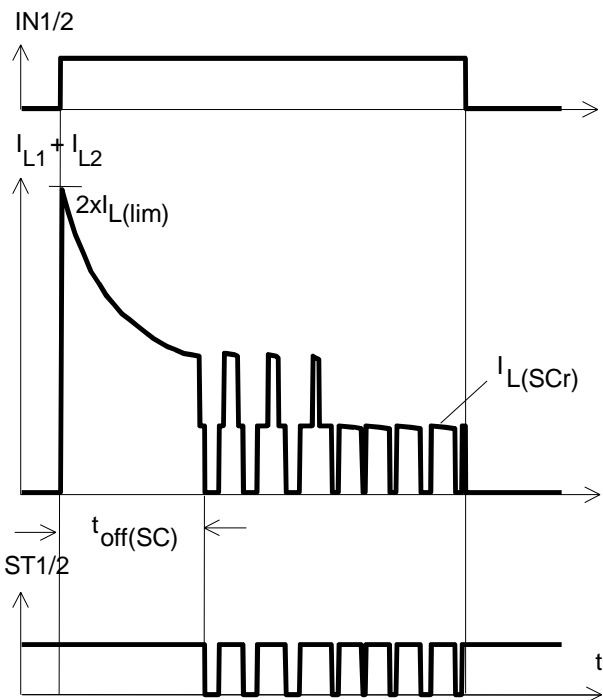
*) if the time constant of load is too large, open-load-status may occur

Figure 3a: Turn on into short circuit: shut down by overtemperature, restart by cooling



Heating up of the chip may require several milliseconds, depending on external conditions

Figure 3b: Turn on into short circuit: shut down by overtemperature, restart by cooling (two parallel switched channels 1 and 2)



ST1 and ST2 have to be configured as a 'Wired OR' function ST1/2 with a single pull-up resistor.

Figure 4a: Overtemperature: Reset if $T_j < T_{jt}$

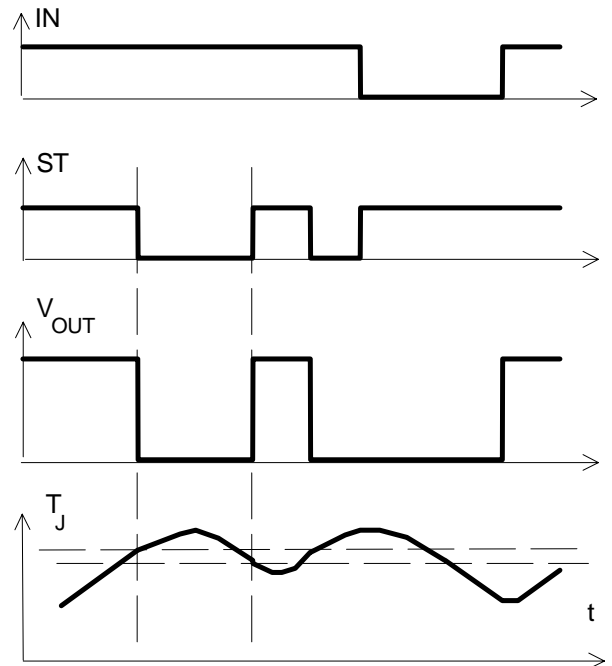
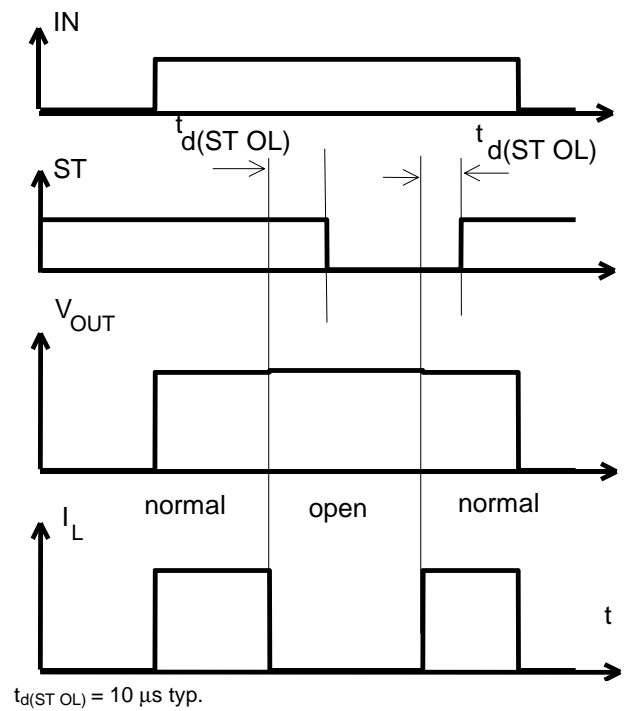


Figure 5a: Open load: detection in ON-state, open load occurs in on-state



$t_{d(ST OL)} = 10 \mu s$ typ.

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