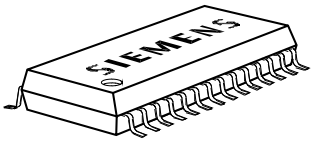
Data Sheet

1 Overview



P-DSO-28-14

1.1 Features

- Quad D-MOS switch driver
- Free configurable as bridge or quad-switch
- Optimized for DC motor management applications
- Low $_{DS\ ON}$: 70 mΩ high-side switch, 40 mΩ low-side switch (typical values @ 25 °C)
- Maximum peak current: typ. 15 A @ 25 °C
- Very low quiescent current: typ. 5 µA @ 25 °C
- Small outline, enhanced power P-DSO-package
- Load and GND-short-circuit-protection
- Operates up to 40 V
- Status flag diagnosis
- Overtemperature shut down with hysteresis
- Internal clamp diodes
- Isolated sources for external current sensing
- Under-voltage detection with hysteresis
- PWM frequencies up to 50 kHz

Type	Ordering Code	Package
BTS 7710 G	Q67007-A9399	P-DSO-28-14

1.2 Description

The **BTS 7710 G** is part of the **TrilithIC** family containing three dies in one package: One double high-side switch and two low-side switches. The drains of these three vertical DMOS chips are mounted on separated leadframes. The sources are connected to individual pins, so the **BTS 7710 G** can be used in H-bridge- as well as in any other configuration. The double high-side is manufactured in **SMART SIPMOS**® technology which combines low $_{DS\ ON}$ vertical DMOS power stages with CMOS control circuitry. The high-side switch is fully protected and contains the control and diagnosis circuitry. To achieve low $_{DS\ ON}$ and fast switching performance, the low-side switches are manufactured in **S-FET** logic level technology. The equivalent standard product is the **BUZ 103 SL**.

In contrast to the **BTS 7710 GP**, which consists of the same chips in an **P-TO263-15** package, the **P-DSO-28-14** package offers a smaller outline and a lower price for applications, which do not need the thermal properties of the **P-TO263-15**.

1.3 Pin Configuration
(top view)

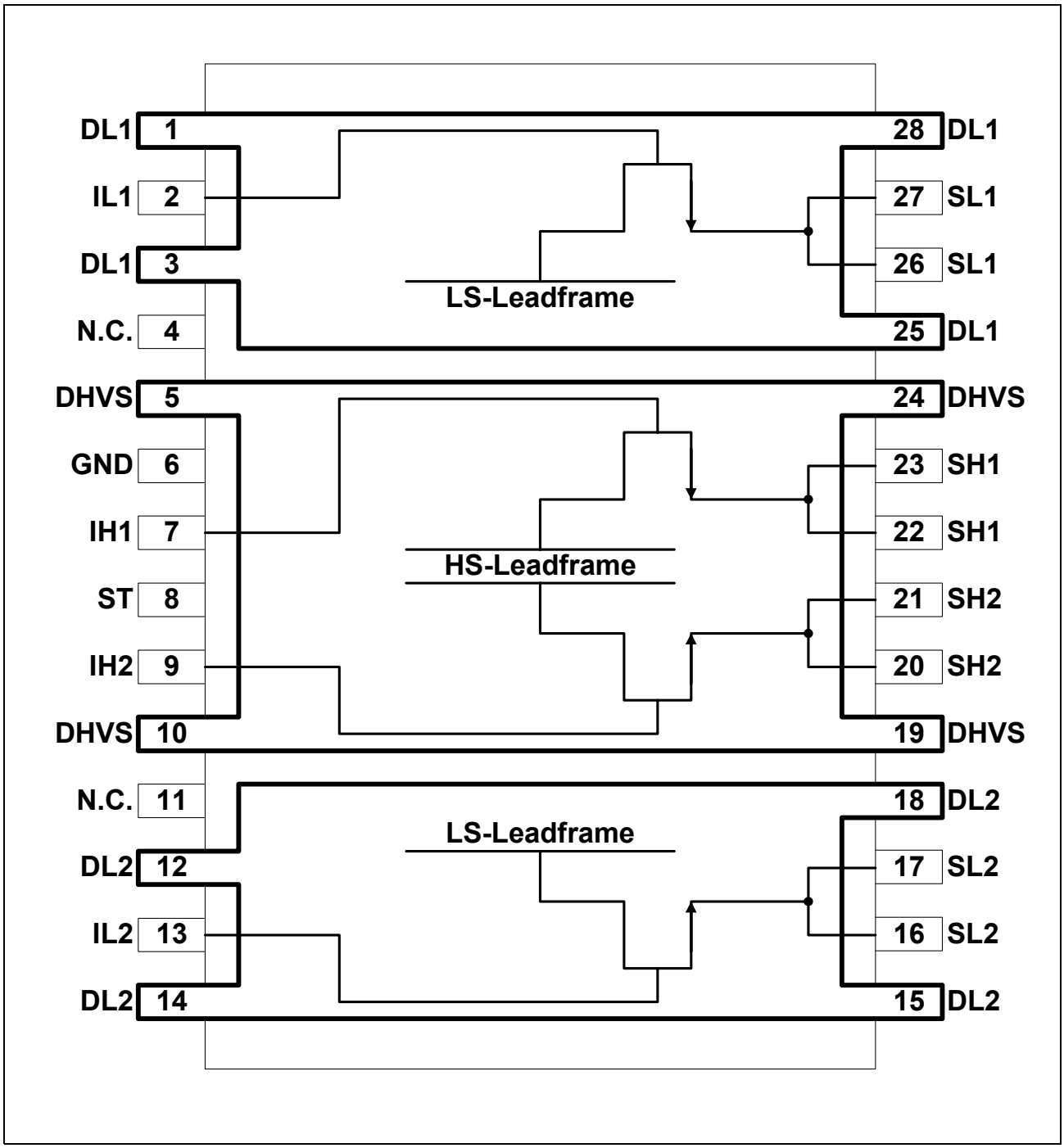


Figure 1

1.4 Pin Definitions and Functions

Pin No.	Symbol	Function
1, 3, 25, 28	**DL1**	**Drain of low-side switch1, leadframe 1** [1)]
2	IL1	Analog input of low-side switch1
4	N.C.	not connected
5, 10, 19, 24	**DHVS**	**Drain of high-side switches and power supply voltage, leadframe 2** [1)]
6	GND	Ground
7	IH1	Digital input of high-side switch1
8	ST	Status of high-side switches; open Drain output
9	IH2	Digital input of high-side switch2
11	N.C.	not connected
12, 14, 15, 18	**DL2**	**Drain of low-side switch2, leadframe 3** [1)]
13	IL2	Analog input of low-side switch2
16,17	**SL2**	**Source of low-side switch2**
20,21	**SH2**	**Source of high-side switch2**
22,23	**SH1**	**Source of high-side switch1**
26,27	**SL1**	**Source of low-side switch1**

[1)] To reduce the thermal resistance these pins are direct connected via metal bridges to the leadframe.

Pins written in **bold type** need power wiring.

1.5 Functional Block Diagram

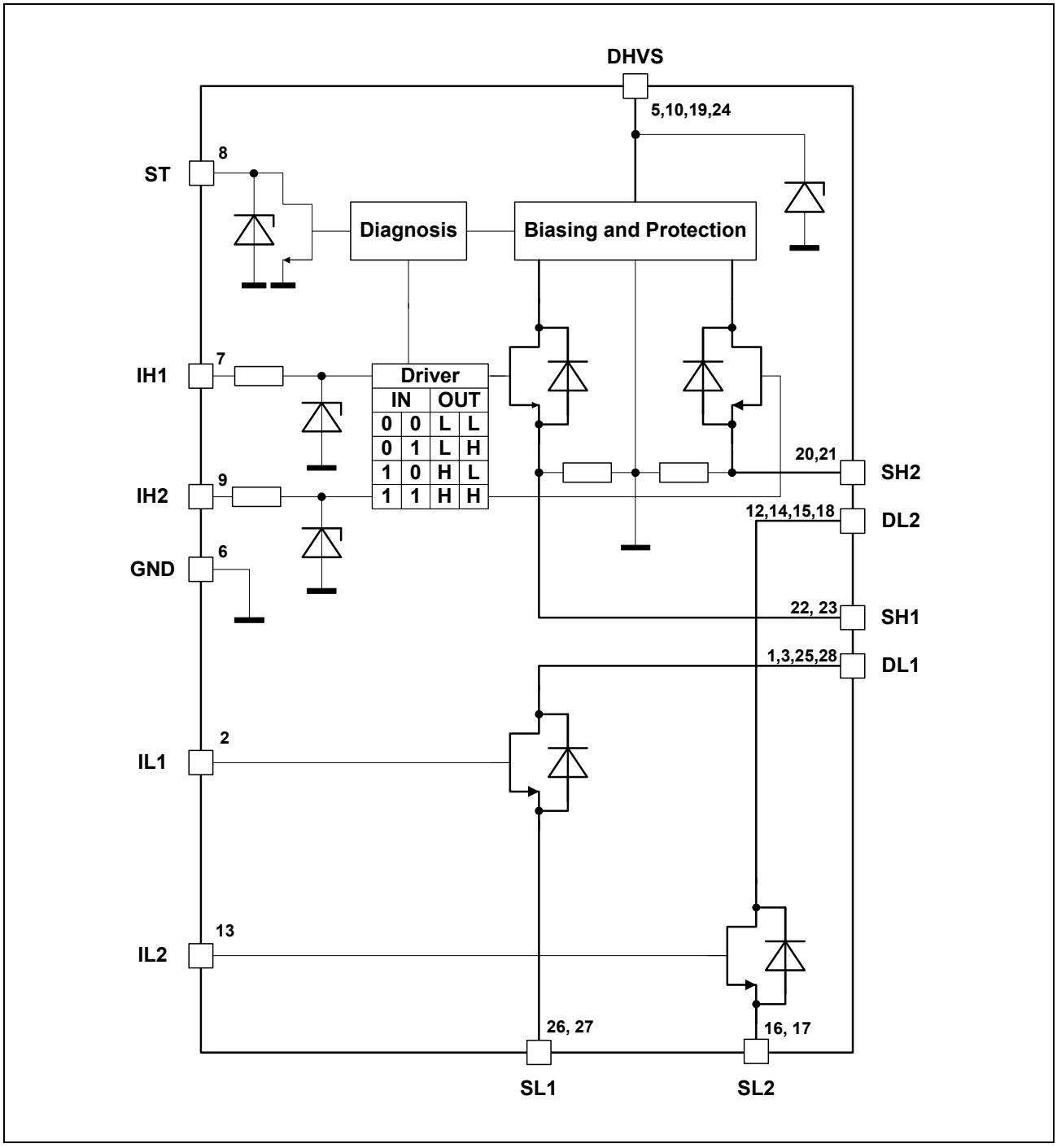


Figure 2
Block Diagram

1.6 Circuit Description

Input Circuit

The control inputs IH1,2 consist of TTL/CMOS compatible Schmitt-Triggers with hysteresis. Buffer amplifiers are driven by these stages and convert the logic signal into the necessary form for driving the power output stages. The inputs are protected by ESD clamp-diodes.

The inputs IL1 and IL2 are connected to the gates of the standard N-channel vertical power-MOS-FETs.

Output Stages

The output stages consist of an low $_{DS\ ON}$ Power-MOS H-bridge. In H-bridge configuration, the D-MOS body diodes can be used for freewheeling when commutating inductive loads. If the high-side switches are used as single switches, positive and negative voltage spikes which occur when driving inductive loads are limited by integrated power clamp diodes.

Short Circuit Protection

The outputs are protected against

– output short circuit to ground
– overload (load short circuit).

An internal OP-Amp controls the Drain-Source-Voltage by comparing the DS-Voltage-Drop with an internal reference voltage. Above this trippoint the OP-Amp reduces the output current depending on the junction temperature and the drop voltage.

In the case of overloaded high-side switches the status output is set to low.

Overtemperature Protection

The high-side switches incorporate an overtemperature protection circuit with hysteresis which switches off the output transistors and sets the status output to low.

Undervoltage-Lockout (UVLO)

When $_{S}$ reaches the switch-on voltage $_{UVON}$ the IC becomes active with a hysteresis. The High-Side output transistors are switched off if the supply voltage $_{S}$ drops below the switch off value $_{UVOFF}$.

Status Flag

The status flag output is an open drain output with Zener-diode which requires a pull-up resistor, c.f. the application circuit on page 14. Various errors as listed in the table “Diagnosis” are detected by switching the open drain output ST to low. A open load detection is not available. Freewheeling condition does not cause an error.

2 Truthtable and Diagnosis (valid only for the High-Side-Switches)

Flag	IH1	IH2	SH1	SH2	ST	Remarks
	Inputs		Outputs			
Normal operation; identical with functional truth table	0 0 1 1	0 1 0 1	L L H H	L H L H	1 1 1 1	stand-by mode switch2 active switch1 active both switches active
Overtemperature high-side switch1	0 1	X X	L L	X X	1 0	 detected
Overtemperature high-side switch2	X X	0 1	X X	L L	1 0	 detected
Overtemperature both high-side switches	0 X 1	0 1 X	L L L	L L L	1 0 0	 detected detected
Undervoltage	X	X	L	L	1	not detected

Inputs:
0 = Logic LOW
1 = Logic HIGH
X = don’t care

Outputs:
Z = Output in tristate condition
L = Output in sink condition
H = Output in source condition
X = Voltage level undefined

Status:
1 = No error
0 = Error

3.1 Absolute Maximum Ratings (cont'd)

– 40 °C < $_j$ < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Thermal Resistances (one HS-LS-Path active)					
LS-junction case	$_{thjC\ L}$	–	20	K/W	measured to pin 3 or 12
HS-junction case	$_{thjC\ H}$	–	20	K/W	measured to pin 19
Junction ambient $_{thja} = T_{j(HS)}/(P_{(HS)}+P_{(LS)})$	$_{thja}$	–	60	K/W	device soldered to reference PCB with 6 cm^2 cooling area
ESD Protection (Human Body Model acc. MIL STD 883D, method 3015.7 and EOS/ ESD assn. standard S5.1 - 1993)					
Input LS-Switch	$_{ESD}$	–	0.5	kV	
Input HS-Switch	$_{ESD}$	–	1	kV	
Status HS-Switch	$_{ESD}$	–	2	kV	
Output LS and HS-Switch	$_{ESD}$	–	8	kV	all other pins connected to Ground

Note: Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

3.2 Operating Range

– 40 °C < $_j$ < 150 °C

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	$_S$	$_{UVOFF}$	42	V	After $_S$ rising above $_{UVON}$
Input voltages HS	$_{IH}$	– 0.3	15	V	–
Input voltages LS	$_{IL}$	– 0.3	20	V	–
Output current	$_{ST}$	0	2	mA	–
Junction temperature	$_j$	– 40	150	°C	–

Note: In the operating range the functions given in the circuit description are fulfilled.

3.3 Electrical Characteristics (cont'd)

$I_{SH1} = I_{SH2} = I_{SL1} = I_{SL2} = 0$ A; – 40 °C < T_j < 150 °C; 8 V < V_S < 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Output stages						
Inverse diode of high-side switch; Forward-voltage	V_{FH}	–	0.8	1.2	V	I_{FH} = 3A
Inverse diode of lowside switch; Forward-voltage	V_{FL}	–	0.8	1.2	V	I_{FL} = 3 A
Static drain-source on-resistance of highside switch	$R_{DS\ ON\ H}$	–	70	90	mΩ	I_{SH} = 1 A T_j = 25 °C
Static drain-source on-resistance of lowside switch	$R_{DS\ ON\ L}$	–	40	50	mΩ	I_{SL} = 1 A; V_{IL} = 5 V T_j = 25 °C
Static path on-resistance	$R_{DS\ ON}$	–	–	260	mΩ	$R_{DS\ ON\ H}$ $R_{DS\ ON\ L}$ I_{SH} = 1 A;
Short Circuit of highside switch to GND						
Initial peak SC current	$I_{SCP\ H}$	15	18	20	A	T_j = – 40 °C
Initial peak SC current	$I_{SCP\ H}$	13	15	17	A	T_j = + 25 °C
Initial peak SC current	$I_{SCP\ H}$	9	11	13	A	T_j = + 150 °C
Short Circuit of highside switch to V_S						
Output pull-down-resistor	R_O	8	15	35	kΩ	V_{DSL} = 3 V
Thermal Shutdown						
Thermal shutdown junction temperature	$T_{j\ SD}$	155	180	190	°C	–
Thermal switch-on junction temperature	$T_{j\ SO}$	150	170	180	°C	–
Temperature hysteresis	Δ	–	10	–	°C	$\Delta = T_{jSD} - T_{jSO}$

3.3 Electrical Characteristics (cont'd)

$_{SH1}$ = $_{SH2}$ = $_{SL1}$ = $_{SL2}$ = 0 A; – 40 °C < $_{j}$ < 150 °C; 8 V < $_{S}$ < 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Status Flag Output ST of highside switch						
Low output voltage	$_{ST\,L}$	–	0.2	0.6	V	$_{ST}$ = 1.6 mA
Leakage current	$_{ST\,LK}$	–	–	10	µA	$_{ST}$ = 5 V
Zener-limit-voltage	$_{ST\,Z}$	5.4		–	V	$_{ST}$ = 1.6 mA
Switching times of highside switch						
Turn-ON-time; to 90% $_{SH}$	$_{ON}$	–	75	160	µs	R_{Load} = 12 Ω $_{S}$ = 12 V
Turn-OFF-time; to 10% $_{SH}$	$_{OFF}$	–	60	160	µs	R_{Load} = 12 Ω $_{S}$ = 12 V
Slew rate on 10 to 30% $_{SH}$	$_{ON}$	–	–	1.5	V µs	R_{Load} = 12 Ω $_{S}$ = 12 V
Slew rate off 70 to 40% $_{SH}$	$_{OFF}$	–	–	2.0	V µs	R_{Load} = 12 Ω $_{S}$ = 12 V
Switching times of low-side switch						
Turn-ON delay time; $_{IL}$ = 5V; $_{G}$ = 7Ω	d_ON_L	–	9	14	ns	resistive load $_{SL}$ = 3 A; $_{S}$ = 30 V
Switch-ON time; $_{IL}$= 5V; $_{G}$ = 7Ω	ON_L	–	25	40	ns	resistive load $_{SL}$ = 3 A; $_{S}$ = 30 V
Switch-OFF delay time; $_{IL}$= 5V; $_{G}$ = 7Ω	d_OFF_L	–	36	55	ns	resistive load $_{SL}$ = 3 A; $_{S}$ = 30 V
Switch-OFF time; $_{IL}$= 5V; $_{G}$ = 7Ω	OFF_L	–	22	33	ns	resistive load $_{SL}$ = 3 A; $_{S}$ = 30 V

Note: switching times are guaranteed by design

3.3 Electrical Characteristics (cont'd)

$_{SH1}$ = $_{SH2}$ = $_{SL1}$ = $_{SL2}$ = 0 A; – 40 °C < $_{j}$ < 150 °C; 8 V < $_{S}$ < 18 V
unless otherwise specified

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Gate charge of lowside switch						
Input to source charge;	$_{IS}$	–	4	6	nC	$_{SL}$ = 3 A; $_{S}$ = 14 V
Input to drain charge;	$_{ID}$	–	10	16	nC	$_{SL}$ = 3 A; $_{S}$ = 14 V
Input charge total;	$_{I}$	–	28	43	nC	$_{SL}$ = 3 A; $_{S}$ = 14 V $_{IL}$ = 0 to 10 V
Input plateau voltage;	$_{(plateau)}$	–	2.75	-	V	$_{SL}$ = 3 A; $_{S}$ = 14 V
Note: switching times and input charges are guaranteed by design						
Control Inputs of highside switches IH 1, 2						
H-input voltage	$_{IH\ High}$	–	–	2.5	V	–
L-input voltage	$_{IH\ Low}$	1	–	–	V	–
Input voltage hysterese	$_{IH\ HY}$	–	0.3	–	V	–
H-input current	$_{IH\ High}$	15	30	60	µA	$_{GH}$ = 5 V
L-input current	$_{IH\ Low}$	5	–	20	µA	$_{GH}$ = 0.4 V
Input series resistance	$_{I}$	2.7	4	5.5	kΩ	–
Zener limit voltage	$_{IH\ Z}$	5.4	–	–	V	$_{GH}$ = 1.6 mA
Control Inputs IL1, 2						
Gate-threshold-voltage	$_{IL\ th}$	0.9	1.7	2.2	V	$_{DL}$ = 1 mA

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $_{A}$ = 25 °C and the given supply voltage.

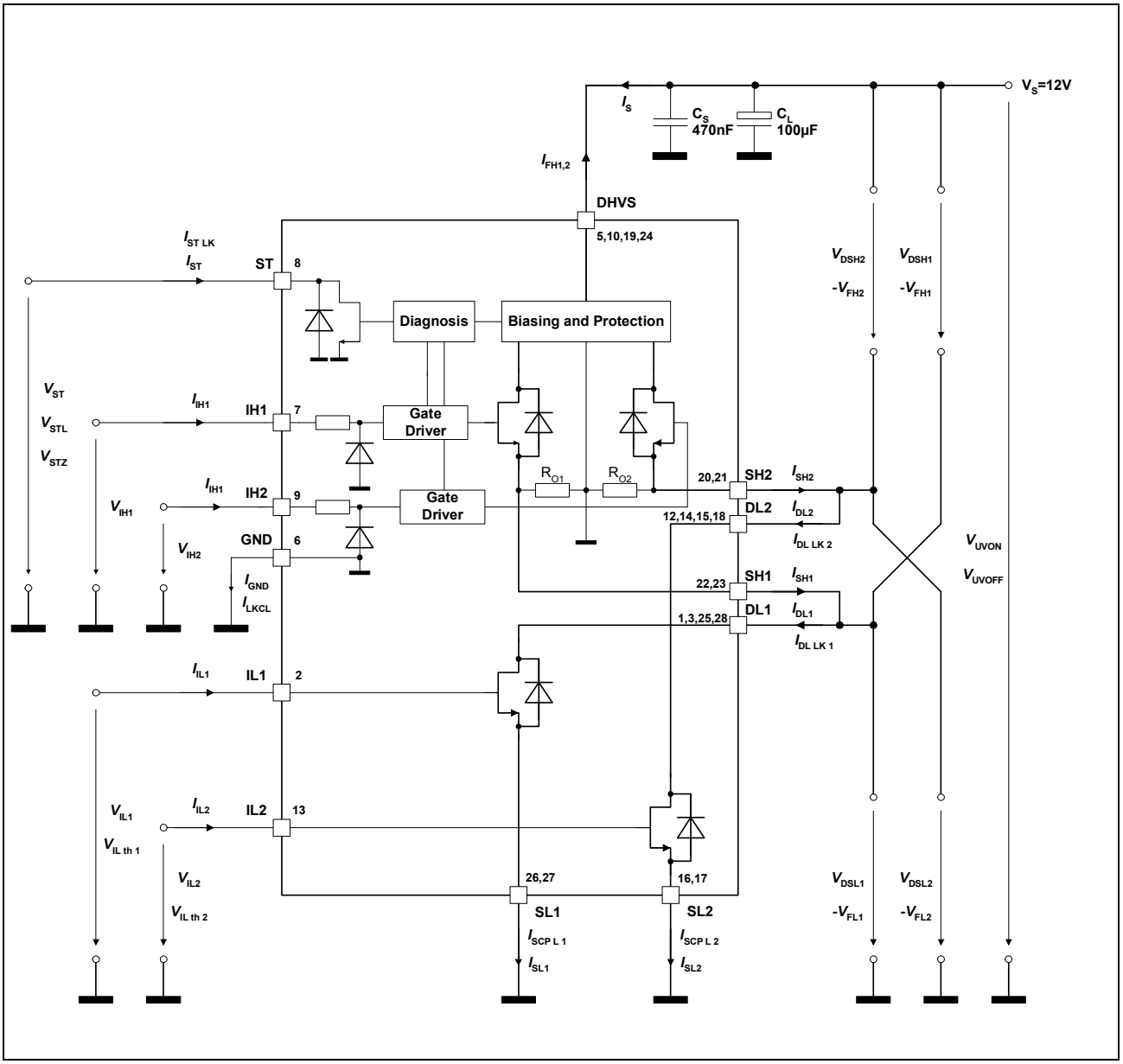


Figure 3
Test Circuit

HS-Source-Current	Named during Short Circuit	Named during Leakage-Cond.
SH1,2	SCP H	DL LK

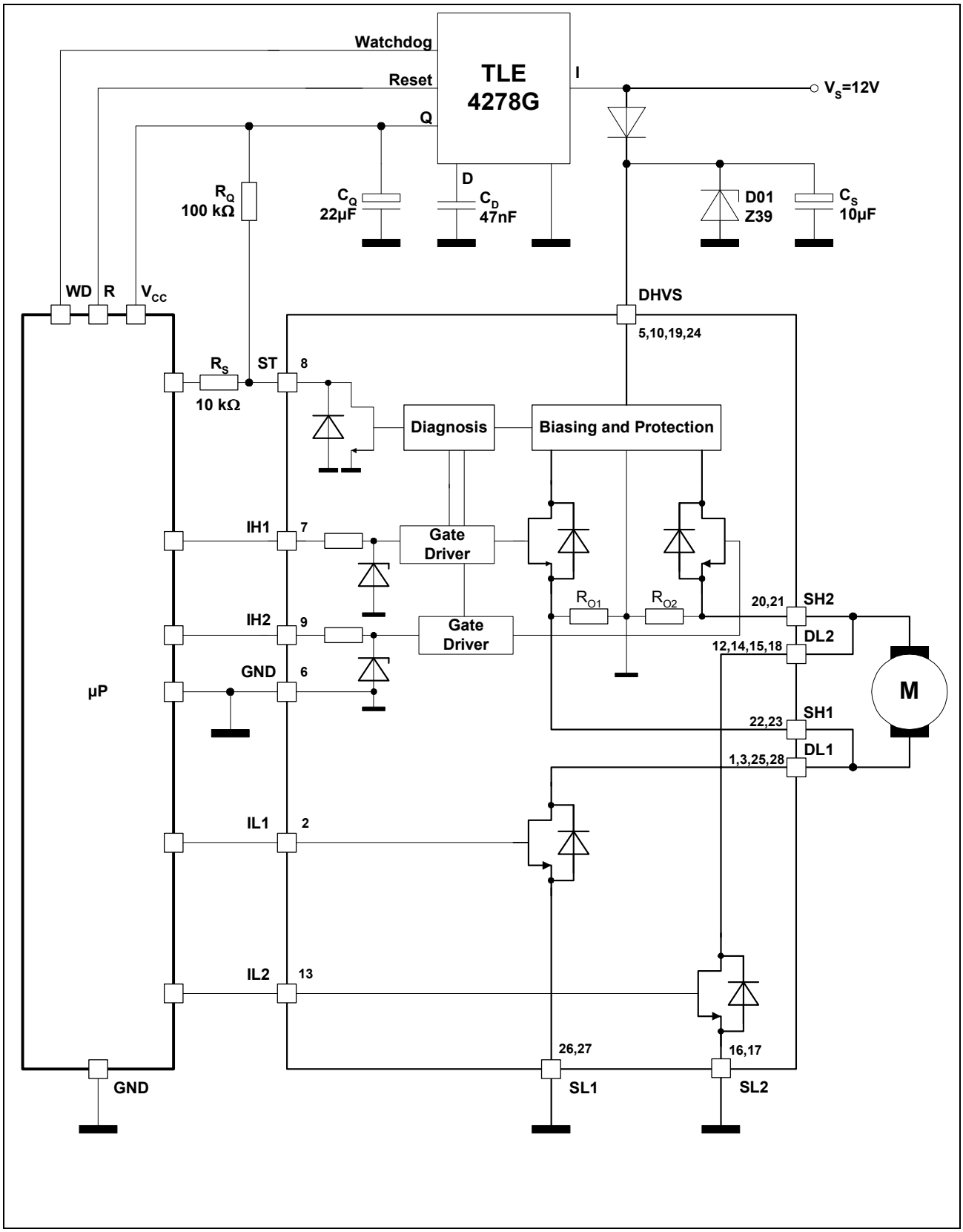


Figure 4
Application Circuit

+0.150.35

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